

Neuro-Fuzzy Five-level Cascaded Multilevel Inverter for Active Power Filter

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Abstract—This paper presents an investigation of five-Level Cascaded H-bridge(CHB) inverter as Active Power Filter in Power System (PS) for compensation of reactive power and harmonics. The advantages of CHB inverter are low harmonic distortion, reduced number of switches and suppression of switching losses. The Active Power Filter helps to improve the power factor and eliminate the Total Harmonics Distortion (THD) drawn from a Non-Linear Diode Rectifier Load (NLDRL). The D-Q reference frame theory is used to generate the reference compensating currents for Active Power Filter while Neuro-Fuzzy controller(NFC) is used for capacitor dc voltage regulation. A CHB Inverter is considered for shunt compensation of a 11 kV distribution system. Finally a level shifted PWM (LSPWM) technique adopted to investigate the performance of CHB Inverter. The results are obtained through Mat lab / Simulink .

Index Terms— Active power filter(APF), Five-level cascade inverter, level shifted pulse width modulation(LSPWM), neuro-fuzzy controller(NFC),total harmonic distortion(THD), harmonics.

I. INTRODUCTION

The widespread increase of non-linear loads nowadays, significant amounts of harmonic currents are being injected into power systems. Harmonic currents flow through the power system impedance, causing voltage distortion at the harmonic currents' frequencies. The distorted voltage waveform causes harmonic currents to be drawn by other loads connected at the point of common coupling (PCC). The existence of current and voltage harmonics in power systems increases losses in the lines, decreases the power factor and can cause timing errors in sensitive electronic equipments. The use of grid connected power electronic converters to improve power quality in power distribution systems represents the best solution, in terms of performance and stability, for the elimination of harmonic distortion, power factor correction, balancing of loads, and voltage regulation.

The most common example of this type of equipment is the active power filter (APF) which has two main configurations: the shunt connected active power filter is placed in parallel with a non-linear load (NLL) and controlled to cancel the current harmonics created by it; its dual, the

series active power filter, is employed for voltage correction and is connected in line with the NLL [1-7]. Power quality (PQ) is the key to successful delivery of quality product and operation of an industry. The term PQ means to maintain purely sinusoidal current waveform in phase with a purely sinusoidal voltage waveform. The deteriorating quality of electric power is mainly because of current and voltage harmonics due to wide spread application of static power converters, zero and negative sequence components originated by the use of single phase and unbalanced loads, reactive power, voltage sag, voltage swell, flicker, voltage interruption etc. The cascade multilevel inverter based active power filter is suitable for power line conditioning in the power distribution network[8]. A hierarchical neuro-fuzzy current control scheme for a shunt active power filter improve the performance[9].

The power conversion strategy called multilevel inversion decreases the total harmonic distortion (THD) by obtaining the output voltage in steps and bringing the output closer to a sine wave [10]. Producing an approximate sinusoidal voltage from multiple levels of dc voltages, normally obtained from capacitor voltage sources is the common objective of multilevel inverters [11]. A multi-pulse inverter like 6-pulse or 12-pulse inverter achieves harmonic as well as reactive power (VAR) compensation through numerous voltage-source inverters interconnected in a zigzag manner by means of transformers [12]. Flexible ac transmission systems, renewable energy sources, uninterruptible power supplies and active power filters are some power electronics applications in which multilevel inverters are important [13]. Multi-level inverters (MLI) have emerged as a successful and realistic solution for power increase and harmonics reduction of AC waveform [14].

This paper presents various issues in design of Neuro-Fuzzy controller and level shifted carrier (LSPWM) technique are used to obtain switching logic for Active power filter. The performance of these controllers is demonstrated with linear resistive-inductive (R-L) loads through simulation results using Power System toolboxes (PST) of Simulink / MATLAB.

II. DESIGN OF MULTILEVEL INVERTER BASED ACTIVE POWER FILTER

A. Active power filter

The increased severity of harmonic pollution in power networks has attracted the attention of power electronics and power system engineers to develop dynamic and adjustable solutions to the power quality problems. Such equipments, generally known as active filters [15], are also called active power line conditioners. To effectively compensate the line current harmonics, the active filter controller should be designed to meet the following three goals:

1. extract harmonic currents and inject compensating current;
2. maintain a constant dc capacitor voltage;
3. avoid generating or absorbing reactive power with fundamental frequency components.

The shunt APF shown in Fig.1 has the structure of a multilevel voltage source inverter connected to the line by an inductance L_f rated at about 5% of the filter power. The dc link storage component is a capacitor, usually of larger value than in a standard power inverter [8].

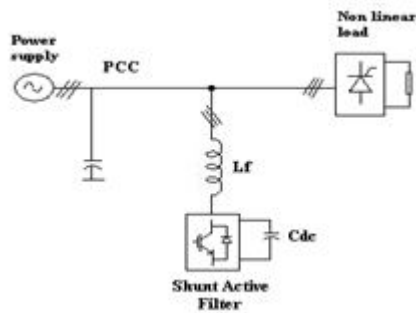


Figure 1. Shunt active power filter

B. Control for dc link voltage

The aim of the control scheme is to maintain constant voltage magnitude at the point where a sensitive load under system disturbances is connected. The control system only measures the rms voltage at the load point, i.e., no reactive power measurements are required. The VSC switching strategy is based on a sinusoidal PWM technique which offers simplicity and good response. Since custom power is a relatively low-power application, PWM methods offer a more flexible option than the fundamental frequency switching methods favored in FACTS applications. Apart from this, high switching frequencies can be used to improve on the efficiency of the converter, without incurring significant switching losses.

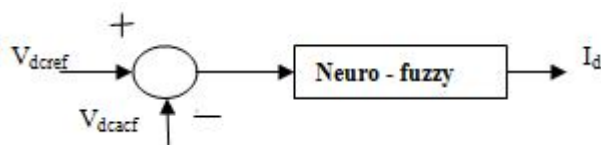


Figure.2 Neuro-fuzzy control for reactive power compensation

The controller input is an error signal obtained from the reference voltage and the rms terminal voltage measured. Such error is processed by a neuro-fuzzy controller; the output is the angle δ , which is provided to the PWM signal generator as shown in Fig.2. It is important to note that in this case, of indirectly controlled converter, there is active and reactive power exchange with the network simultaneously. The neuro-fuzzy controller processes the error signal and generates the required angle to drive the error to zero, i.e. the load rms voltage is brought back to the reference voltage.

C. Neuro-Fuzzy Controller

Neuro fuzzy system gives the switching angles and frequency value. By using this value the harmonic contents present in the system are eliminated. The overall process takes place in proposed method is shown in Fig.4. Feed back controller used here is to calculate voltage error values in the system. This voltage error values is given as the input to neuro fuzzy system. In the feedback controller, the voltage values are calculated from the voltage waveform for different time values. From the reference waveform voltage values at different time values are taken as reference voltage value. Then for different time values, the voltage values are taken from the harmonics waveform and compared with the reference waveform. The voltage error values are calculated using the equation given below.

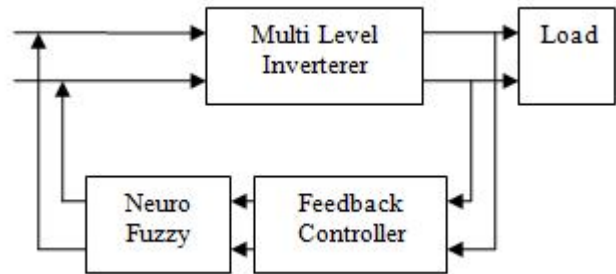


Figure 3. Proposed method

$$V_{error} = V_{ref} - V_h \quad (1)$$

where V_{ref} is the voltage value of the system without harmonics.

After calculating the voltage error values, next step is to generate training dataset for training neuro fuzzy system. Generating training dataset is one of the most important processes because based on the training dataset only the neuro fuzzy system will be trained.

The training dataset generated for training neuro fuzzy system consists of n input variables and $s + 1$ output variables. Here, n stands for number of voltage values taken for generating dataset, s is the total number of dataset generated, is the switching angle and $s + 1$ stands for number of switching angles. The dataset generated for our proposed method is shown below.

$$D = \begin{bmatrix} V_{t11} & V_{t12} & \dots & V_{t1n} \\ V_{t21} & V_{t22} & \dots & V_{t2n} \\ \vdots & \vdots & \ddots & \vdots \\ V_{tr1} & V_{tr2} & \dots & V_{tr1} \end{bmatrix} \begin{bmatrix} \theta_{11} & \theta_{12} & \dots & \theta_{1n} \\ \theta_{21} & \theta_{22} & \dots & \theta_{2n} \\ \vdots & \vdots & \ddots & \vdots \\ \theta_{r1} & \theta_{r2} & \dots & \theta_{r1} \end{bmatrix} \quad (2)$$

By using the above dataset, neuro fuzzy system is trained. The neuro fuzzy operation is explained briefly in the below sections.

The steps for training the neural network are

Step 1: Initialize the input weight of each neuron.

Step 2: Apply a training dataset to the network.

Here Y_1, Y_2, \dots, Y_n are the input to the network and

Z_1, Z_2, \dots, Z_{s+1} are the output of the network.

$$Z_1 = \sum_{r=1}^n W_{2r1} Z_1(r) \quad (3)$$

$$Z_2 = \sum_{r=1}^n W_{2r2} Z_2(r) \quad (4)$$

$$\text{where, } Z_{s+1} = \sum_{r=1}^n W_{2r(s+1)} Z_{s+1}(r) \quad (5)$$

$$Z(r) = \frac{1}{1 + \exp(-w_{11r} \cdot \sum_{k=1}^n Y(k))} \quad (6)$$

Eqn 12, 13, 14 & 15 represents the activation function performed in the output and input layer respectively.

Step 3: Adjust the weights of all neurons.

Step 4: For each set of voltage values, select the switching angle and frequency.

Step 5: Select the best switching angle and frequency.

After completion of training, neuro fuzzy is used for practical application. After completion of training neuro fuzzy system the next step is to eliminate the harmonic contents in the system. First voltage error values are calculated using the equation 3. By giving voltage error values as input to the neuro fuzzy system, it gives corresponding frequency and switching angles as output. By applying this frequency and switching angle values to the system the harmonic contents present in the system are eliminated. The frequency and switching angle are substituted in the equation given below.

$$V(t) = V_h \cdot \sin(h \cdot 2\pi \cdot f_f \cdot t) \quad (7)$$

where, f_f is the frequency obtained from neuro fuzzy system.

$$V_h = \frac{4V_{dc}}{h\pi} \sum_{j=1}^S \cos(h\theta_j) \quad (8)$$

where, θ_j is the switching angles obtained from neuro

fuzzy system and h is the harmonic order.

By substituting equation 5 in 1 we get the output dc voltage. The harmonics content eliminated or not is calculated using the below condition.

$$H_{eli} = \begin{cases} V_{ref}(t) = V(t); \text{harmonics eliminated} \\ V_{ref}(t) \neq V(t); \text{harmonics present} \end{cases}$$

D. Cascaded H-Bridge Multilevel Inverter

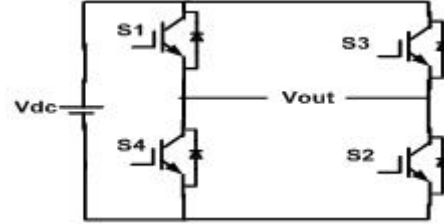


Figure.4 Circuit of the single cascaded H-Bridge Inverter

Fig.4 shows the circuit model of a single CHB inverter configuration. By using single H-Bridge we can get 3 voltage levels. The number of output voltage levels of CHB is given by $2n+1$ and voltage step of each level is given by $V_{dc}/2n$, where n is number of H-bridges connected in cascaded. The switching table is given in Table.I.

TABLE I. SWITCHING TABLE OF SINGLE CHB INVERTER

Switches Turn ON	Voltage Level
S1,S2	V_{dc}
S3,S4	$-V_{dc}$
S4,D2	0

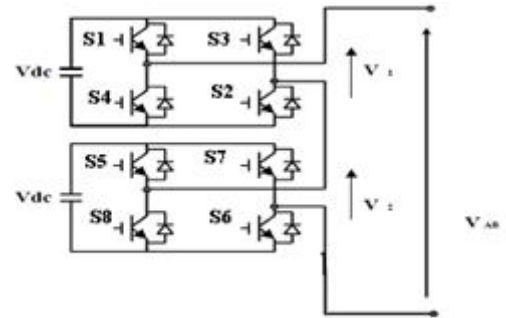


Figure.5. Block diagram of 5-level CHB inverter model

The switching mechanism for 5-level CHB inverter is shown in table-II.

Table II. Switching table for 5-level CHB Inverter

Switches Turn On	Voltage Level
S1, S2	V_{dc}
S1,S2,S5,S6	$2V_{dc}$
S4,D2,S8,D6	0
S3,S4	$-V_{dc}$
S3,S4,S7,S8	$-2V_{dc}$

III. DESIGN OF SINGLE H-BRIDGE CELL

A. Device Current

The IGBT and DIODE currents can be obtained from the load current by multiplying with the corresponding duty cycles. Duty cycle, $d = \frac{1}{2}(1 + K_m \sin \omega t)$, Where, m = modulation index $K = +1$ for IGBT, -1 for Diode. For a load current given by

$$I_{ph} = \sqrt{2} I \sin(\omega t - \phi) \quad (9)$$

Then the device current can be written as follows.

$$i_{device} = \frac{\sqrt{2}}{2} I \sin(\omega t - \phi) x (1 + k_m \sin \omega t) \quad (10)$$

The average value of the device current over a cycle is calculated as

$$i_{avg} = \frac{1}{2\pi} \int_{\phi}^{\pi+\phi} \frac{\sqrt{2}}{2} I \sin(\omega t - \phi) x (1 + k_m \sin \omega t) d\omega t \quad (11)$$

B. IGBT Loss Calculation

IGBT loss can be calculated by the sum of switching loss and conduction loss. The conduction loss can be calculated by,

$$(P_{on(IGBT)} = V_{ceo} * I_{avg(igbt)} + I_{rms(igbt)}^2 * \Gamma_{ceo} \quad (12)$$

$$I_{avg(igbt)} = \sqrt{2} I \left[\frac{1}{2\pi} + \frac{m}{g} \cos \phi \right] \quad (13)$$

$$I_{rms(igbt)} = \sqrt{2} I \left[\frac{1}{g} + \frac{m}{3\pi} \cos \phi \right] \quad (14)$$

Values of V_{ceo} and r_{ceo} at any junction temperature can be obtained from the output characteristics (Ic vs. Vce) of the IGBT as shown in Fig .6.

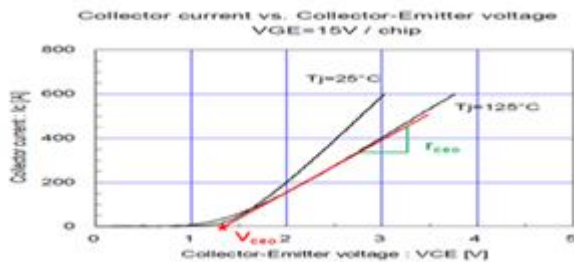


Figure.6. IGBT output characteristics

The switching losses are the sum of all turn-on and turn-off energies at the switching events

$$E_{sw} = E_{on} + E_{off} = a + bI + cI^2 \quad (15)$$

Here V_{DC} is the actual DC-Link voltage and V_{nom} is the DC-Link Voltage at which E_{sw} is given. Switching losses are calculated by summing up the switching energies.

Here 'n' depends on the switching frequency.

$$P_{sw} = \frac{1}{T_0} \sum_n E_{sw}(i) \quad (16)$$

Here 'n' depends on the switching frequency.

After considering the DC-Link voltage variations, switching losses of the IGBT can be written as follows.

$$P_{sw(IGBT)} = f_{sw} \quad (17)$$

So, the sum of conduction and switching losses is the total losses given by

$$P_{T(IGBT)} = P_{on(IGBT)} + P_{sw(IGBT)} \quad (18)$$

C. Diode Loss Calculation

The DIODE switching losses consist of its reverse recovery losses; the turn-on losses are negligible.

$$E_{rec} = a + bI + cI^2 \quad (19)$$

$$P_{sw(DIODE)} = f_{sw} \quad (20)$$

So, the sum of conduction and switching losses gives the total DIODE losses.

$$P_{T(DIODE)} = P_{on(DIODE)} + P_{sw(DIODE)} \quad (21)$$

The total loss per one switch (IGBT+DIODE) is the sum of one IGBT and DIODE loss.

$$P_T = P_{T(IGBT)} + P_{T(DIODE)} \quad (22)$$

D. Thermal Calculations

The junction temperatures of the IGBT and DIODE are calculated based on the device power losses and thermal resistances. The thermal resistance equivalent circuit for a module is shown in fig-7. In this design the thermal calculations are started with heat sink temperature as the reference temperature. So, the case temperature from the model can be written as follows.

$$T_c = P_T R_{th(c-h)} + T_h \quad (23)$$

Here $R_{th(c-h)}$ = Thermal resistance between case and heat sink

$$P_T = TotalPowerLoss(IGBT + DIODE) \quad (24)$$

IGBT junction temperature is the sum of the case temperature and temperature raise due to the power losses in the IGBT.

$$T_{j(IGBT)} = P_{T(IGBT)} R_{th(j-c)IGBT} + T_c \quad (25)$$

The DIODE junction temperature is the sum of the case temperature and temperature raise due to the power losses in the DIODE.

$$T_{j(DIODE)} = P_{T(DIODE)} R_{th(j-c)DIODE} + T_c \quad (26)$$

The above calculations are done based on the average power losses computed over a cycle. So, the corresponding thermal calculation gives the average junction temperature. In order to make the calculated values close to the actual values, transient temperature values are to be added to the average junction temperatures.

E. Level Shifted Carrier PWM (LSCPWM) Technique

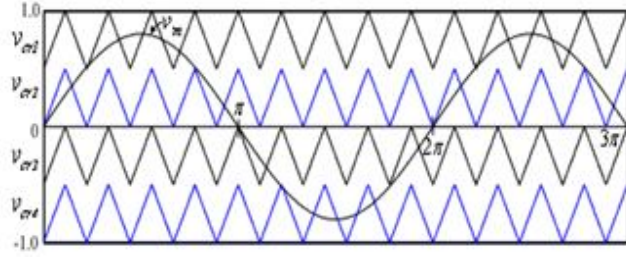


Figure-7 Level shifted carrier PWM (IPD)

Fig.7. shows the Level shifted carrier pulse width modulation. An m-level Cascaded H-bridge inverter using level shifted modulation requires $(m-1)$ triangular carriers, all having the same frequency and amplitude. For PID modulation, the multilevel converter with multilevel requires $(m1)$ triangular carriers with same amplitude and frequency. The frequency modulation index ' m_f ' which can be expressed as

$$m_f = f_{cr} / f_m \quad (27)$$

where f_m is modulating frequency and f_{cr} are carrier waves frequency.

The amplitude modulation index ' ma ' is defined by

$$m_a = V_m / V_{cr(m-1)} \text{ for } 0 \leq ma \leq 1 \quad (28)$$

Where V_m is the peak value of the modulating wave and V_{cr} is the peak value of the each carrier wave [1]. The amplitude modulation index, ma is 1 and the frequency modulation index, m_f is 6. The triggering circuit is designed based on the three phase sinusoidal modulation waves V_a , V_b , and V_c . Three of the sine wave sources have been obtained with same amplitude and frequency but displaced 120° out of the phase with each others. For carriers wave sources block parameters, the time values of each carrier waves are set to $[0 \ 1/600 \ 1/300]$ while the outputs values are set according to the disposition of carrier waves. After comparing, the output signals of comparator are transmitted to the IGBTs. Figures 8, 9 and 11 shows the waveforms based on three schemes of level shifted multilevel modulations: (a) in phase disposition (IPD) fig.7, where all carriers are in phase; (b) alternative phase opposite disposition (APOD) Fig.8, where all carriers are alternatively in opposite disposition; and (c) phase opposite disposition (POD) fig.9, where all carriers above zero reference are in phase but in opposition with those below the zero reference [1]. Out of IPD, APOD and POD; we found that, IPD give better harmonic performance.

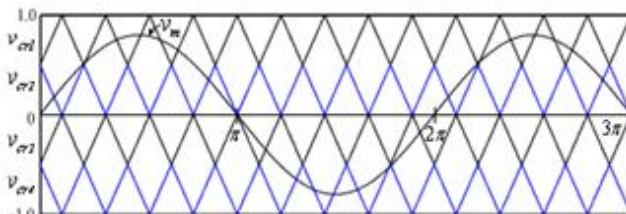


Figure. 8. Alternative phase opposite disposition (APOD)

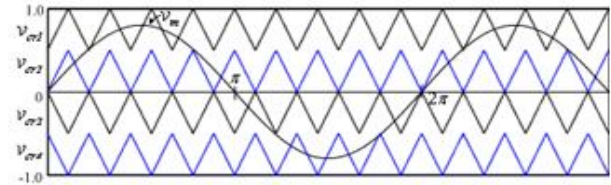


Fig. 9 phase opposite disposition (POD)

IV. MATLAB/SIMULINK MODELING AND SIMULATION RESULTS

Fig.10. shows the Matab / Simulink power circuit model of APF. It consists of five blocks named as source block, non linear load block, control block, APF block and measurements block. The system parameters for simulation study are source voltage of 11kv, 50Hz AC supply, DC bus capacitance 1550iF, Inverter series inductance 10mH, Source resistance of 0.1ohm and inductance of 0.9mH. Load resistance and inductance are chosen as 30mH and 60ohms respectively.

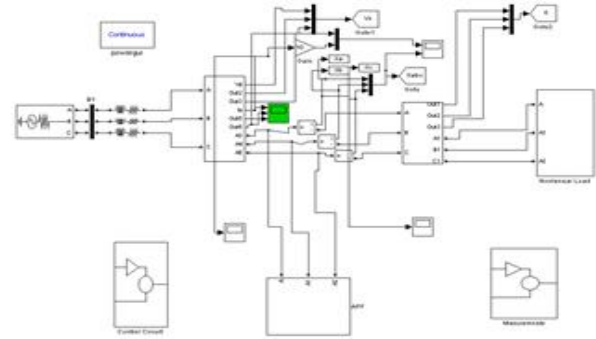


Fig-10 Matlab/Simulink power circuit model of APF

Level shifted carrier PWM technique results

Fig. 11. shows the phase-A voltage of five level output of level shifted carrier PWM inverter.

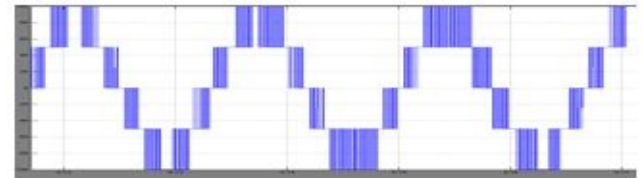


Figure.11. five level LSCPWM output

Fig.12. shows the three phase source voltages, three phase source currents and load currents respectively without APF. It is clear that without APF load current and source currents are same.

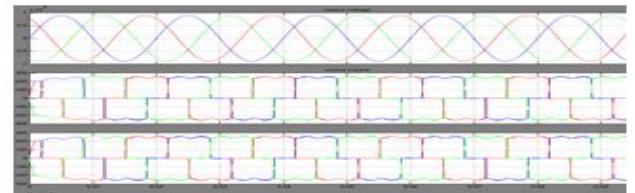


Figure.12. Source voltage, current and load current without APF

Fig.13 shows the three phase source voltages, three phase source currents and load currents respectively with APF. It is clear that with APF even though load current is non sinusoidal source currents are sinusoidal.

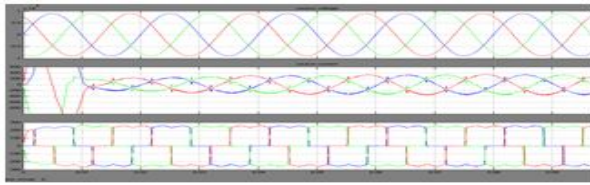


Figure.13. Source voltage, current and load current with APF

Fig.14. shows the DC bus voltage with respect to time. The DC bus voltage is regulated to 11kv by using Neuro-Fuzzy controller.

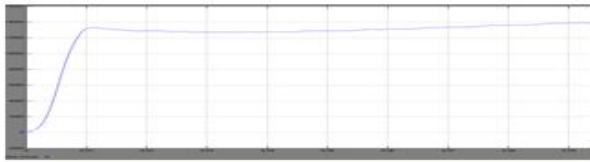


Figure.14. DC Bus Vooltage

Fig.15 shows the phase-A source voltage and current, even though the load is non linear RL load the source power factor is unity.

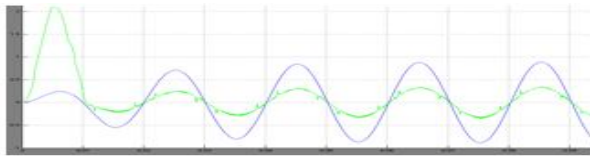


Figure.15. Phase-A source voltage and current

Fig.16. shows the harmonic spectrum of Phase –A Source current without APF. The THD of source current without APF is 29.48 %.

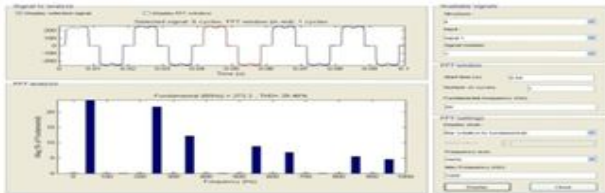


Figure.16 Harmonic spectrum of Phase-A Source current without APF

Fig.17. shows the harmonic spectrum of Phase –A Source current with APF. The THD of source current with APF is 7%.

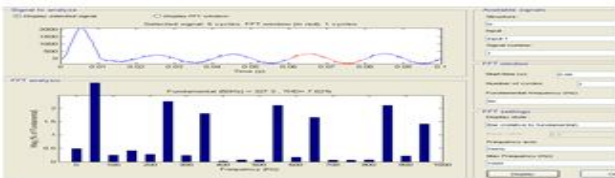


Figure.17. Harmonic spectrum of Phase-A Source current with APF

CONCLUSION

The Mathematical model for single H-Bridge inverter is developed which can be extended to multi H-Bridge. A Active Power Filter with five-level CHB Multilevel inverter is investigated for LSCPWM. The source voltage, load voltage, source current, load current, power factor and THD simulation results under non-linear loads are investigated. Finally Matlab/Simulink based model is developed and simulation

results are presented.

REFERENCES

- [1] A. Ajami and S. H. Hosseini, "Implementation of a Novel Control Strategy for Shunt Active Filter," ECTI Transactions On Electrical Eng., Electronics, And Communications. Vol.4, No.1, pp. 40-46, February 2006.
- [2] M. Ghandchi, A. Ajami and M. Moeini, "A Simple and Low Cost Control Strategy for Multilevel Shunt Active Filters," in Proceeding of International Conference on Control, Automation and Systems 2008 in COEX, Seoul, Korea. pp. 14-17, October 2008.
- [3] P. Zanchetta, M. Sumner, M. Marinelli and F. Cupertino, "Experimental modeling and control design of shunt active power filters," Control Engineering Practice, Vol.17, pp. 1126 – 1135, May 2009.
- [4] M.George, K. P. Basu, "Three-Phase Shunt Active Power Filter," American Journal of Applied Sciences, Vol. 5, No. 8,pp. 909-916, 2008..
- [5] M.C. Benhabib, S. Saadate, " New control approach for four-wire active power filter based on the use of synchronous reference frame", Electric Power System Research, Vol.73 , pp. 353–362, 2005.
- [6] C. Yanbo, Z. Fudan, K.W. E. Cheng, "Shunt Active Power Filter – Simulink Simulation and DSP-based International Conference on Power Electronics Systems and Applications, pp. 120-125, 2006.
- [7] G. Zhoua, B. Wub, D. Xuc, "Direct power control of a multilevel inverter based active power filter", Electric Power System Research, Vol.77 , pp. 284–294, 2007.
- [8] Karuppanan and Kamalakanth mahapatra, "PI/PID and fuzzy logic controlled cascaded voltage source inverter based active power filter for power line conditioners", Wseas Transactions on power systems, Issue 4, Vol.6 ,October 2011, pp. 100–109.
- [9] K.Cagatay Bayindir,M.ugras Cuma,Mehmet Tumay, "Hierarchical neuro-fuzzy current control for a shunt active power filter", Neural computing and applications ,volume 15, issue 3-4,pp 223-238, June 2006.
- [10] S. Jeevananthan, "Evolutionary Computing Based Area Integration PWM Technique for Multilevel Inverters", Journal of Electrical Systems, Vol.3, No.2, P.p:61-72, 2007.
- [11] Eswaran Chandra Sekaran, Ponna Nadar, Anbalagan and Chelliah Palanisamy, "Analysis and Simulation of a New Shunt Active Power Filter Using Cascaded Multilevel Inverter ", Journal of Electrical Engineering, Vol. 58, No. 5,pp. 241–249,2007.
- [12] P.Palanivel, Subhransu Sekher, Dash, "Phase Shifted Carrier Pulse Width Modulation for Three Phase Multilevel Inverter to Minimize THD and Enhance Output Voltage Performance", Journal of Electrical Systems, Vol.6, No. 2, pp. 1-13, June 2010.
- [13] A. Hussein. Attia, M. El- Metwally and Osama M. Fahmy, "Harmonic Distortion Effects and Mitigation in Distribution Systems", Journal of American Science, Vol. 6, No. 10, pp. 173-183, 2010.
- [14] A. F. Zobaa, "Practical Solutions for Harmonics Problems Produced in the Distribution Networks", Journal of Electrical Systems, Vol. 2, No.1 pp.13-28, 2006.
- [15] P.Mattavelli, "Aclosed-loop selective harmonic mpensation for active filters", IEEE Trans. Ind. Appl., vol. 37, no. 1, pp. 81–89, Jan./Feb. 2001.